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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,359	01/21/2004	Yoshihiro Saeki	030712-21	8709

22204 7590 06/28/2006

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EXAMINER	
HA, NATHAN W	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,359	SAEKI ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In this case, the mentioned claims recite that the second circuit area includes a circuit, which is subject to noise. It is unclear how the circuit subject to noise. Does it generate noises due to parasitic capacitance of the wires? Or does it reduce the noises therein? It seems that this limitation is inherently disclosed since every IC includes parasitic capacitance, which occurs due to high scale VLSI circuits. This capacitance generates noise, or crossing, which is a well-known phenomenon. Otherwise, please clarify. And for the examination purposes, the Office presumes that the subject to noise is generated by the parasitic capacitance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawaishi (US 6,798,071, newly cited.)

In regard to claims 1-2 and 10, in fig. 3, Kawaishi discloses a semiconductor device comprising:

a first semiconductor chip 1;

a second semiconductor chip 2 which mounted on the first chip;

a first electrode group 32 located on the first chip so as to be arranged on an outer periphery of the second chip;

a second electrode group 33 located on the first chip and arranged along an outer periphery of the first chip, wherein the second electrode group surround the first electrode group;

a third electrode group, not numbered, located on the second chip;

a plurality of first wires 6, fig. 6, for electrically connecting the first electrode group and the third electrode group; and

external connection terminals, not numbered, located around the first semiconductor chip and electrically connected to the second electrode group,

wherein the first chip has a first circuit area on which the second chip mounted and a second circuit area which positioned between the first electrode group and the second electrode group, and wherein the second area includes a circuit, , or the delay circuit, which prevents crossing therein. See also, col. 6, lines 60-66.

In regard to claim 3, wherein the external connection terminals are conductive leads 3;

the plurality of leads are arranged along the outer periphery of the first semiconductor chip at positions separate from the first semiconductor chip by a predetermined distance; and

the second electrode and the leads are electrically connected to each other by a plurality of second wires 7, fig. 2.

In regard to claims 4 and 11, Kawaishi further discloses wherein a size of the second semiconductor chip is smaller than that of the first semiconductor chip. Fig. 3.

In regard to claims 5, 13, and 20, Kawaishi further discloses wherein the first semiconductor chip and the second semiconductor chip are sealed with a resin 10, fig. 1.

In regard to claims 6 and 14, see the above discussions regarding to claim 3, and the wires also encapsulated in the resin, fig. 3.

In regard to claim 7, wherein the first semiconductor chip is formed on a support, not numbered, see fig. 3.

In regard to claim 8, Kawaishi discloses that the first and second groups are located on the periphery of the first chip. Fig. 3.

In regard to claim 9, the third group is located along the outer periphery of the second chip, fig. 3.

In regard to claims 12, 17, and 19, a relay circuit is analog circuit.

In regard to claim 15, see the discussion regarding to claim 3.

In regard to claims 16 and 18, the central circuit area can occupy outside of the perimeter of the second chip area since the first chip is significantly larger than the second chip. Fig. 3.

Response to Arguments

5. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nathan Ha
June 20, 2006